FVTX Detector

FVTX Closeout Report

[Street Address] [City], [State] [Postal Code]
Phone: [Your Phone] Fax: [Your Fax] E-Mail: mbrooks@lanl.gov

Overview

The two Forward Silicon Vertex Trackers (FVTX) for the Pioneering High Energy Nuclear Interaction eXperiment (PHENIX) experiment at the Relativistic Heavy Ion Collider (RHIC) extend the vertex capability of the PHENIX Silicon Vertex Tracker (VTX) to forward and backward rapidities allowing secondary vertex measurement capability in front of the PHENIX muon arms. The FVTX detector project was approved by the DOE Office of Science in March 2008, with first construction funds received in April 2008. Project complete was declared in December 2011 when the full FVTX detector was installed into PHENIX.

The primary technical improvement provided by the FVTX is to allow for the identification of secondary vertices near the original event vertex. With an expected distance of closest approach (DCA) resolution of 200 μm or better at 5 GeV/c, we will see improvement in both tracking from the original vertex as well as through identifying the location of secondary vertices caused by the in-flight decay of particles.

The FVTX is composed of two endcaps, with four silicon mini-strip planes each, covering angles (~10 to 35 degrees) that match the two muon arms. Each silicon plane consists of 48 wedges of mini-strips with 75μm pitch in the radial direction and lengths in the phi direction varying from 3.4 mm at the inner radius to 11.5 mm at the outer radius. The maximum occupancy per strip reached in central Au-Au collisions is approximately 2.8%.

The FVTX has about 0.54 million strips in each forward detector that are read out with Fermi National Accelerator Laboratory (FNAL) FPHX chips, which are wire bonded directly to the mini-strips. This chip provides analog and digital processing with zero-suppression and produces a digital output which is "data-pushed" at 200 Mbps to an intelligent readout board (ROC) containing Field-Programmable Gate Arrays (FPGAs). There the data are extracted and sent via fiber-optic to another readout board (the FEM) in the counting house. On this board, the data are prepared in a standard PHENIX format and sent to PHENIX standard Data Collection Modules (DCMs).

The FVTX detector provides vertex tracking over a large coverage in rapidity ($1.2 < |\eta| < 2.2$) with full azimuthal coverage. This will allow for vertex cuts which separate prompt particles, decay particles from short-lived heavy quark mesons

and decay particles from long-lived light mesons (pions and kaons). In addition, beauty measurements can be made directly via $B \rightarrow J/\psi+X$ by looking for a displaced J/ψ vertex, which will allow charm and beauty contributions to be separated in semi-inclusive single lepton measurements. Therefore, with this device significantly enhanced and qualitatively new data can be obtained. A more robust and accurate measurement of heavy-quark production over a wide kinematical range will be possible. This new reach to forward and backward rapidity complements the central barrel vertex (VTX) silicon detector, which covers $|\eta| < 1.2$.

The precision of the J/ψ and other di-muon measurements in Au-Au collisions are currently limited in part by the large amount of combinatorial background that must be subtracted from under the signal. With added rejection power for muons from pion and kaon decays, the significance of all di-muon measurements will greatly improve. Further improvement in these measurements results from the improved mass resolution, which will be attained because of the more accurate determination of the opening angles of the di-muons. Altogether, these will result in improvements of our current di-muon analyses as well as providing access to several new measurements: separation of ψ' from J/ψ, extraction of Drell-Yan from the di-muon continuum and measurement of upsilons at central rapidity.

Project Expenditures

The cost analysis from the final FVTX quarterly report is shown in Table 1, where the baseline (cost + contingency) for each item is shown along with the final cost, baseline contingencies, and final contingencies. A number of items had final contingencies which were quite different from the project estimates, but overall we ended out with roughly $80k in contingency, part of which was used to purchase some additional extension cables for which we had few spares. We propose to use the remaining funds, some of which have already been converted to operations funds, to purchase additional spare parts for the FVTX detector.

Table 1 Baseline costs compared to final costs for the FVTX project. The Baseline Total cost listed includes contingency, the Estimated Total Cost is actual cost at the end of the project, Baseline Contingency is the portion of the Baseline Total Cost which was contingency, and the Remaining Contingency is the Baseline Total cost minus the final actual costs.

WBS	ITEM	Baseline Total Cost (AY$)	Estimated Total Cost (AY$)	Baseline Contingency (AY$)	Remaining Contingency (AY$)
1.4.1	Wedge Sensors	1118	796	206	323
1.4.2	FPHX Chip	692	545	174	147
1.4.3	HDI	194	431	39	-237
1.4.4	Flex Cables	70	365	9	-295
1.4 Total		2074	2136	428	-62
1.5.1	Fiber	21	22	3	-1
1.5.5	Ancillary	246	273	23	-26
1.5.2	ROC	615	745	139	-130
1.5.3	FEM	578	339	130	240
1.5 Total		1461	1379	295	82
1.6.2	Cage Wedge	174	311	35	-137
1.6.3	Backplane	188	164	38	24
1.6.4	Support Disk	114	118	23	-4
1.6.5	Jigs	80	59	15	21
1.6 Total		555	651	110	-96
1.7	Assembly	42	11	8	31
1.8	Integration	500	451	58	48
1.9	Management	249	174	28	74
Total		790	637	94	153
Grand Total		**4881**	**4803**	**927**	**77**

Project Schedule

The FVTX project control milestones, along with the baseline and actual complete dates are shown in Table 2. The Project Complete date was changed from June 2011 to December 2011 in agreement with DOE when it was clear that

the RHIC shutdown schedule was not going to accommodate such an early complete date. As can be seen in the Milestone table a number of completion dates were later than expected, primarily due to late deliveries of HDIs, extension cables and ROCs, but we still achieved installation into PHENIX in December 2011.

Table 2 FVTX Project Control Milestones along with Baseline and Actual completion dates.

WBS Number	Control Milestone Name	Baseline Date	Actual/ Forecast Date
WBS 1.1	DOE construction funds received	Q3 FY08	Q3 FY08
Accounts open	Accounts open	Q3 FY08	Q3 FY08
WBS 1.6.2.2.2	Review and Approve wedge, disk, cage design	Q3 FY08	Q3 FY08
WBS 1.4.3.2.5	HDI tested	Q3 FY08	Q2 FY09
WBS 1.4.1.2.3	Sensor prototype tested	Q1 FY09	Q1 FY09
WBS 1.4.1.2.5	First prototype wedge assembly	Q1 FY09	Q2 FY09
WBS 1.5.2.2.6	PHENIX system test complete	Q1 FY09	Q3 FY09
WBS 1.5.2.2.8	Review and Approve FEM and ROC	Q2 FY09	Q2 FY11
WBS 1.4.3.3.1	1st Production HDIs Received	Q2 FY10	Q3 FY10
WBS 1.4.1.3.1	Sensor Procurement complete	Q3 FY09	Q3 FY10
WBS 1.4.1.2.6	Wedge assembly test complete	Q4 FY09	Q4 FY09
WBS 1.4.2.5.1	FPHX engineering run complete	Q1 FY10	Q1 FY10
WBS 1. 5.3	ROC and FEM production Complete	Q2 FY10	Q3 FY11
WBS 1.7.1.1	Disk Assembly begins	Q3 FY10	Q1 FY11
WBS 1.7.2.1	First Two ½ Cages Assembled	Q1 FY11	Q4 FY11
WBS 1.7.2.1	Functional Requirements Tests	Q1 FY11	Q4 FY11

	on Bench Begins		
WBS 1.5.5.6	Install ancillary Equipment	Q4 FY10	Q4 FY11
WBS 1.7.1.1	Disk Assembly complete	Q1 FY11	Q4 FY11
WBS 1.7.2.1	½ Cage Assembly finished	Q2 FY11	Q4 FY11
	All FVTX Component Deliverables Completed	Q2 FY11	Q1 FY12
WBS 1.7.5	Verify Functional Requirements on Bench Completed	Q3 FY11	Q1 FY12
WBS 1.7.3	Install into VTX enclosure	Q2 FY11	Q1 FY12
WBS 1.7.3	Project Complete	Q3 FY11	Q1 FY12

Project Deliverables

The functional requirements and component deliverables from our Management Plan are shown in Table 3 and Table 4, along with the performance that we have achieved to date. In the below sections we describe for each deliverable how the "achieved deliverable" was measured and how it compares to the "proposed deliverable".

Table 3 PHENIX FVTX System Functional Requirements.

Requirement	Proposed Deliverable	Achieved Deliverable
Mini strips active	>80%	99%, 90%*
Hit efficiency	>85%	>95%
Radiation length per wedge	< 2.4 %	<2.4%
Detector hit resolution	< 25 μm	25 μm
Random noise hits/chip	<0.1%	~0.02%
Level-1 latency	4 μs	4 μs
Level-1 Multi-Event buffer depth	4 events	4 events
Read-out time	< 40 μs	9 μs
Read-out rate	> 10 kHz	>27 kHz

*99.9% of wedge channels work, 90% can be read out through the full readout chain

**27 kHz can be sustained with maximum number of channels firing. Ordinarily a much higher rate can in principle be sustained.

Mini Strips Active

The number of mini-strips active has been measured in two ways. First, direct communication with wedges can be used to determine if a wedge itself has power and is operational, as long as the slow control communication to the ROC board that the wedge is attached to is functioning. Second, in order for the wedge data to be fully read out, the ROC data fibers, FEM channels and DCM channels in the wedge readout chain must all be operational. If this chain is fully operational for a wedge then the mini strips are said to be active and reading out.

Out of 384 wedges, in the system, we are able to establish communication with all 384 wedges when the slow control fibers were working. From the detector assembly we know that of the 8448 chips in the system, 8 of them were not operational. **This leaves 99.9% of the wedge channels functional.**

During installation and commissioning we had some failures of ROCs which caused some wedges to no longer be able to be read out. Out of the 24 ROCs in the system, we have one ROC that became inoperable when the slow control transceiver on the ROC was damaged during installation and early commissioning. This removes 4% of our detector from the readout. In addition, one ROC data fiber (which covers ¼ of a ROC) was accidentally shorted out when the east and west detector halves were mated and this fiber is no longer working. The ROC associated with this fiber has only been operational during part of the runs and is currently powered down due to worries that we may further damage the ROC if it is powered on. This removes another 4% of our detector from the readout. Finally, we have two more ROCs that are fully functional, but two data fibers cannot be plugged into the boards because of an interference with a support structure member. This interference cannot be resolved until the next shutdown. Together, these two data fibers remove 2% of our detector from the readout. **This leaves 90% of the detector system able to be read out through ROCs.** All FEM and DCM channels are currently operational.

Hit Efficiency

The hit efficiency for the detectors was measured using real p-p data sets and selecting tracks that passed through stations 0,1 and 3 and were in a sector which had a fully functional station 2 wedge (no dead chips, channels). Those tracks were fit to a straight line and the following cuts were placed on the tracks:

- Theta of the track within acceptance of station 2 wedges
- Phi of the track within acceptance of station 2 wedges
- Station 0-1-3- track fit have a residual < +/- 100 μm

The efficiency was then measured to be: (number of tracks which pass these cuts *and* have a hit at station 2 within a small geometric window)/(number of tracks which pass these cuts). The requirement that the tracks must pass through stations 0,1 and 3 limits the radial coverage of the efficiency measurement at station 2, but within this coverage the efficiency that was measured was high, as shown in Figure 1. The drop at small radius and the large fluctuations at larger radii are when we are in the regions of small acceptance of tracks going through all 4 stations and we therefore have very poor statistics there. In the region of reasonable statistics our efficiency is measured to be >95%.

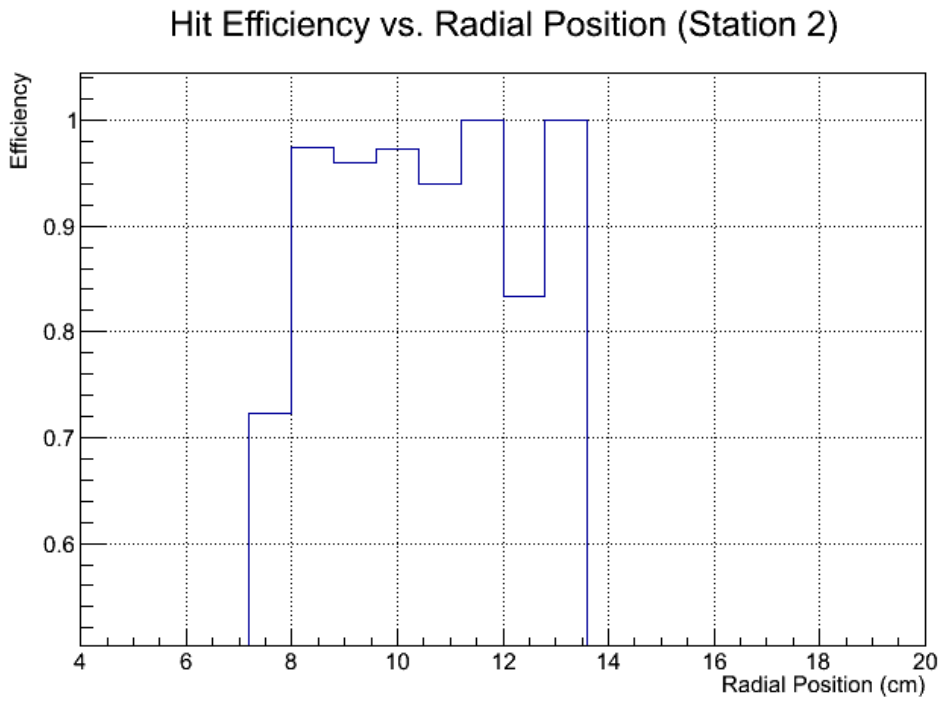

Figure 1 Silicon detector efficiency measured versus radial position on one wedge, at Station 2.

We have also measured the efficiency across the entire detector, including all areas even if a chip is dead or part of the detector is masked off or turned off. The resulting efficiency for one particular run is shown in Figure 2 where we show the station 2 efficiency versus phi for the North arm (top plot) and the South arm (bottom plot). As can be seen in this figure, even when taking into account all dead areas the vast majority of the detector that is powered on and fully operational for the run has efficiency greater than our specification of 80%.

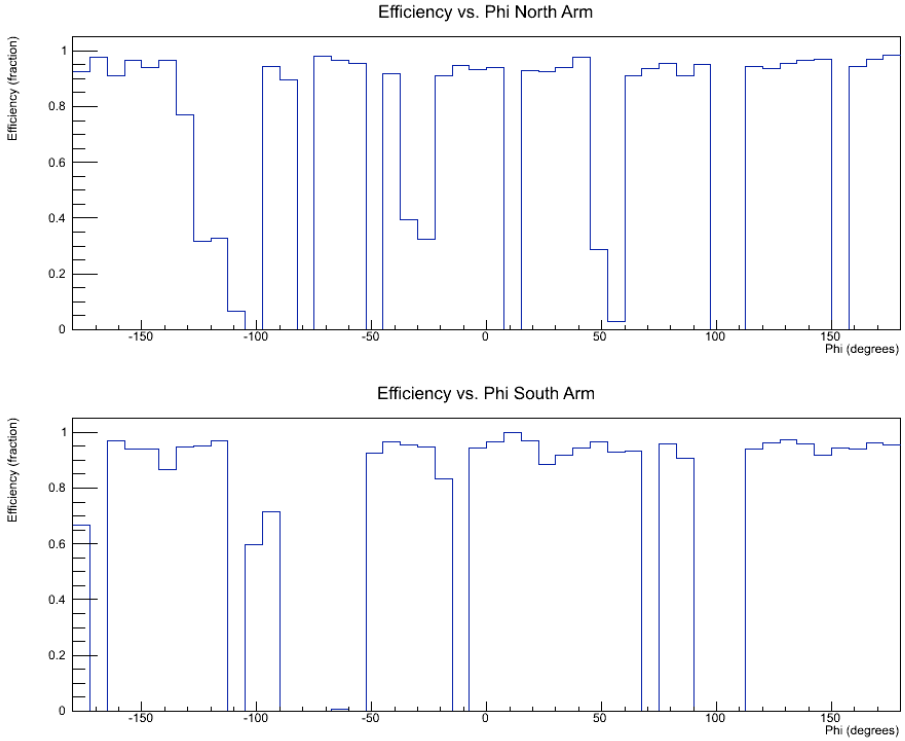

Figure 2 Measured hit efficiency versus phi for the North arm (top) and the South arm (bottom). These hit efficiencies take into account the intrinsic detector efficiency as well as any dead areas of the detector.

Detector Resolution

Similar to the efficiency measurement, the detector resolution was measured by fitting hits in two stations surrounding another station, projecting that fit to the middle station, and taking the difference between the projected position and the measured position in the central station. This produces a residual which is a combination of the projection error from the surrounding stations, some multiple scattering in the intermediate materials, and the intrinsic detector resolution of the station of interest. We reduce the contribution from multiple

scattering by requiring that the residual from the stations that are used in projection is less than +/- 100 μm. Then, if we assume that all stations have the same intrinsic resolution, the projection error can be taken out with simple error propagation and the intrinsic detector resolution becomes ~0.8*residual.

Figure 3 shows the resulting residual versus phi location in the detector for the North and South arms. The projection error has been taken out by multiplying the residual by 0.8 and we have attempted to reduce the multiple scattering contribution with the cut on the residual of the 3 surrounding. Across the detector, the residuals tend to fall between 50 and 100 μms. These residuals, however, also include alignment errors which we have not yet addressed.

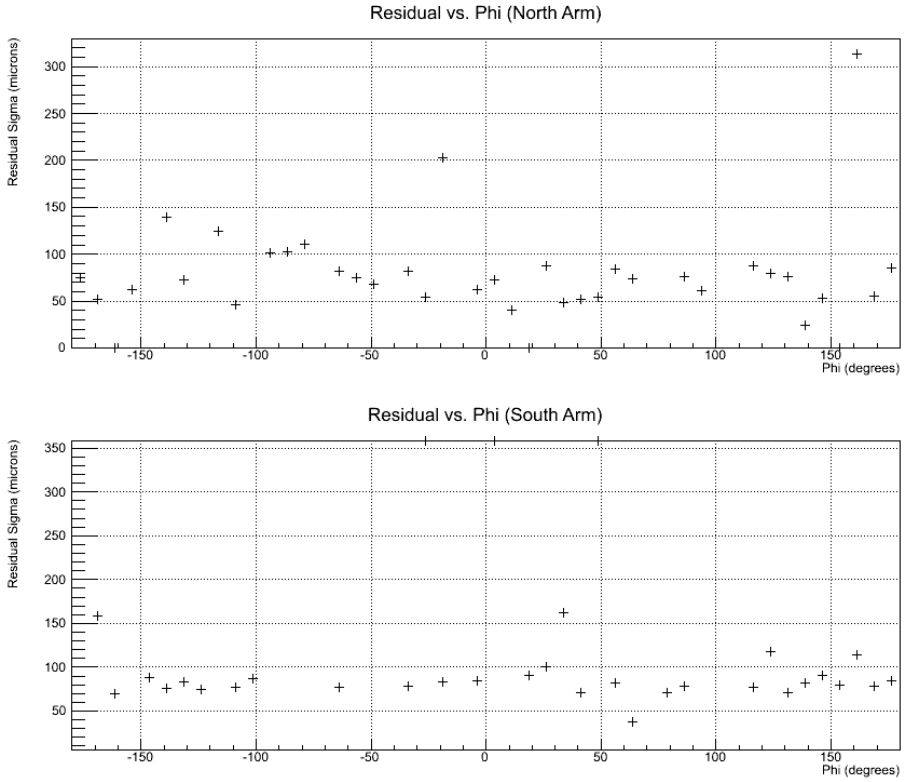

Figure 3 Track residuals at station 2 versus phi for the North arm (top) and the South arm (bottom). The residuals have been calculated by projection a station 0-1-3 track to station 3, taking the difference between the projected and measured position, and reducing this residual by 0.8 to attempt to take out the projection error and just leave the intrinsic detector resolution.

In order to try to remove the misalignment contribution, we have also extracted the residuals for single wedges, with all tracks being required to pass through the same wedge at all 3 stations. An example of one of these residuals is shown in Figure 4. However, we also do not know the momentum distribution of tracks contributing to this residual distribution and therefore do not know the

remaining multiple scattering contributions. To try to understand whether the intrinsic detector resolution is comparable to our expected resolution, we have simulated the same residuals using GEANT and our offline software. Since we expect the majority of tracks going through the detector to be low momentum, we threw muons with p = (0.5, 2.0) GeV and extracted the track residual using the same software as for real data. The resulting residual distribution is shown in Figure 5. The extracted residual is ~49 μm, which is comparable to what we see in real data so we believe that our detector has the expected intrinsic detector resolution of 25 μms which we get from our simulated data.

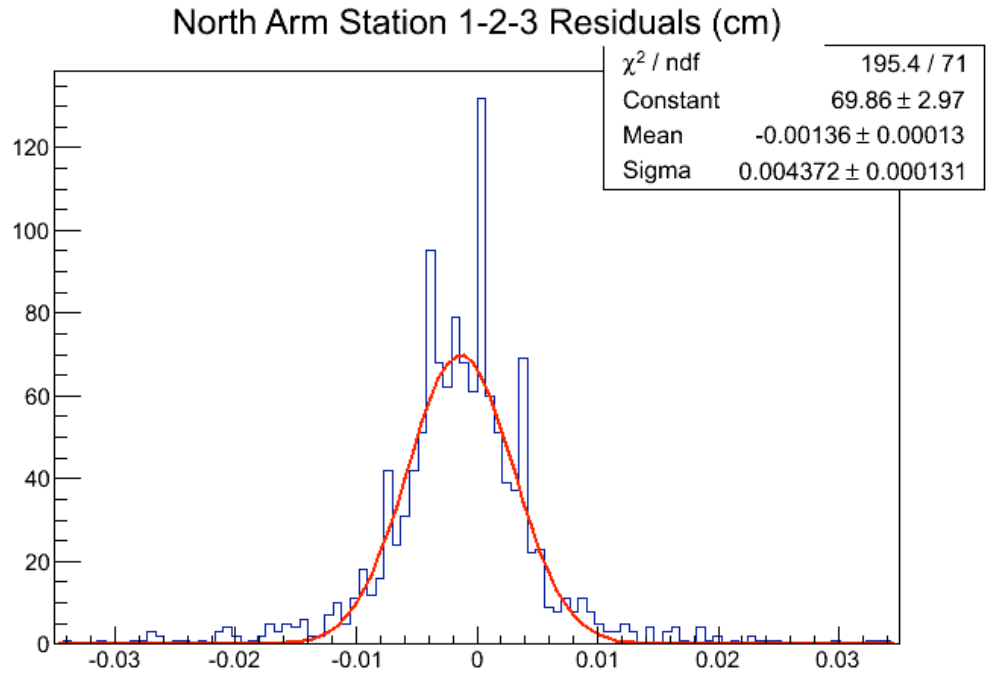

Figure 4 The station 2 residuals for station 1-2-3 tracks, for sector 15 in the North FVTX arm. The extracted sigma for this distribution is approximately 44 μms.

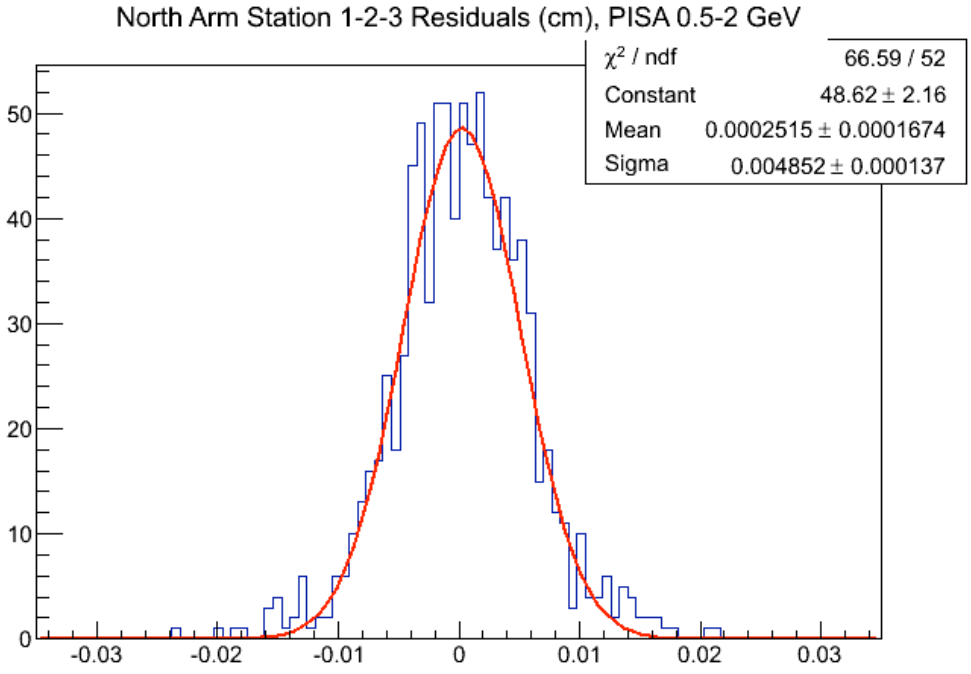

Figure 5 Station 2 track residuals for station 1-2-3 tracks for simulated muons of p = (0.5, 2.0) GeV. The extracted sigma for this distribution is ~49 μm.

Noise Hits

The noise hits/chip specification can be met if the noise levels in the detector are small enough w.r.t the threshold value set for the chips. We have established that this parameter has been met both by making absolute measurements of the noise (in electrons) per channel in the detector and also by looking at the absolute hit rate with no beam. Figure 6 shows the extracted noise value and threshold value for each strip in a particular calibration data set. The calibration data set is collected by pulsing each channel N times for M different input pulser settings from 0 to some maximum value. The threshold is extracted by fitting an error function to the hits versus pulse-height curve and extracting the mid-point of the turn-on. The noise value is the width of that turn-on curve for each channel. The noise and threshold values are converted from pulser input value to electrons by knowing the voltage level per DAC unit and the value of the injection capacitor on the front-end of the FPHX chip. Applying this conversion factor, we get noise values which have an average value of 429 electrons is within our specifications to have noise values of ~500 electrons when we set the threshold to 2500.

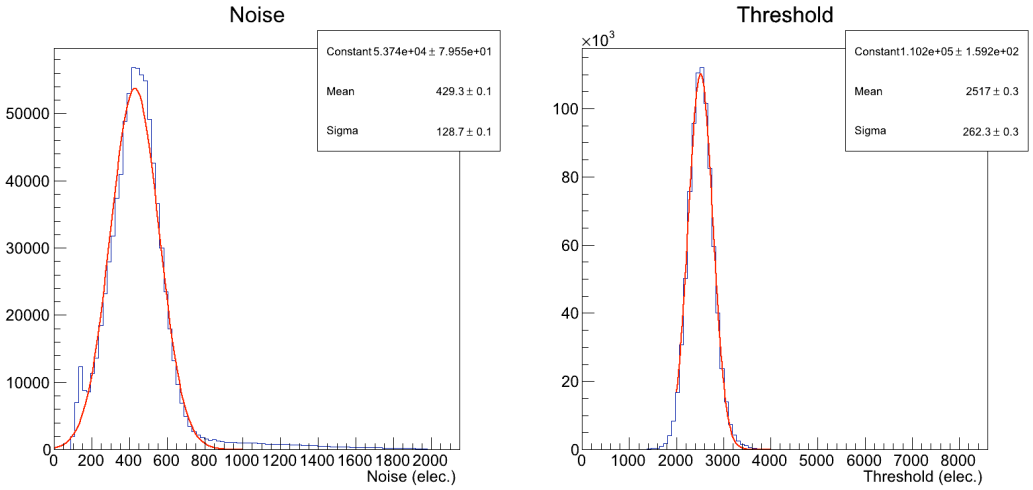

Figure 6 Noise (left-hand plot) and threshold (right-hand plot) extracted from a calibration data set, with one entry per strip that was being calibrated. The average noise value is 429 electrons and the average threshold value is 2517 electrons (consistent with the DAC0=8 setting that was used for the dataset).

Our absolute hit rate has been measured both in stand-alone noise runs and in regular p-p data taking mode. Our noise specification is to have <3.5 hits per wedge per event from noise, to avoid filling our bandwidth with noise hits. This is equivalent to 3.5/(26chips*128channels) = 0.1% hits/chip-channel. Even in the p-p data taking mode you can see in Figure 7, where the average hits/event/wedge is shown for the South arm, that our noise hit rate of <0.8 is well within our specifications of <3.5 hits/event/wedge.

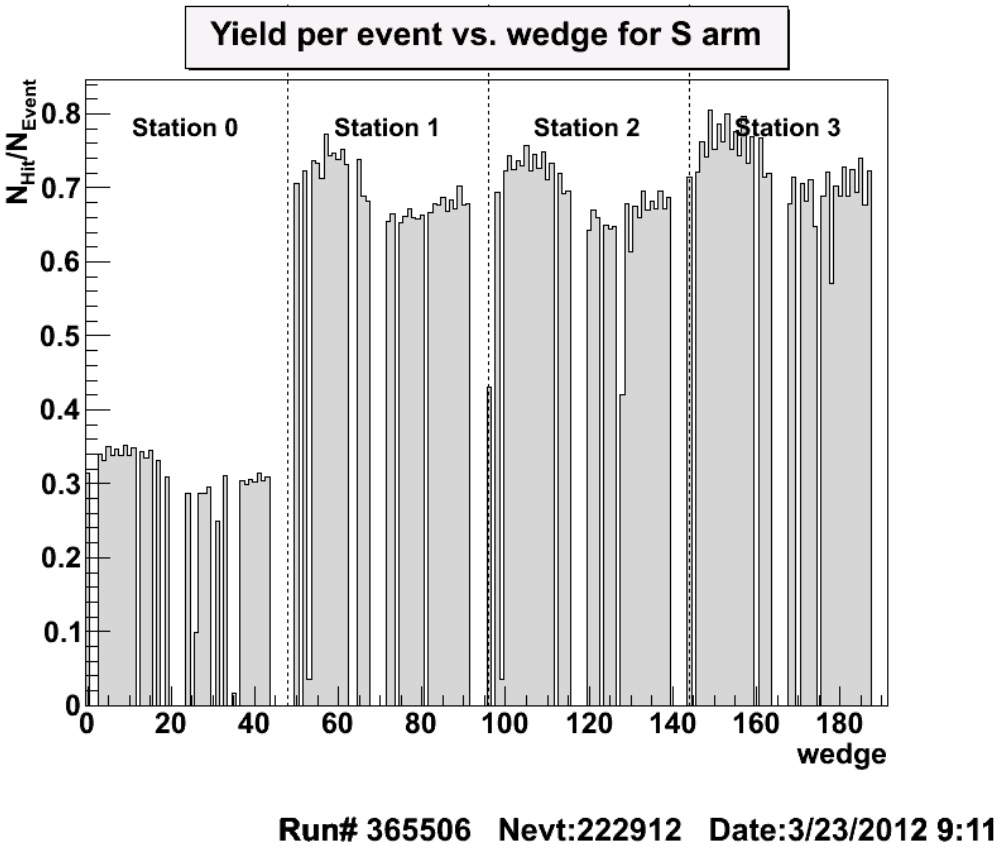

Figure 7 Hits/event/wedge in 500 GeV p-p data taking, for the South FVTX arm.

Lvl-1 Latency, Multi-event Buffering, Readout Time, Readout Rate

The lvl-1 latency specification of <4 μs was set so that the FVTX could have the capability of participating in a PHENIX trigger if we chose to at some point in the future. This specification has been met with the silicon sensor readout specifications which require that 4 hits (maximum number expected in heavy ion collisions) can be latched by the chip within 4 beam clocks (400 ns).

The FPGA code was designed to be able to buffer up to 4 consecutive events worth of data and this design has been achieved and tested.

The readout time for the FEM FPGA code has been fully simulated and is shown to take a maximum of 9 μs for an event that has the maximum number of hits that can be accepted. This meets our specification of <40 μs readout time.

The processing rate of the FEM FPGA code has been fully simulated and is able to sustain a trigger rate of 5 MHz when empty packets are generated (packets which include a PHENIX-standard header and trailer which adds up to seven 16-bit words, but no hits). This maximum trigger rate is reduced by the transfer rate to the DCM and by the addition of hits to the packet size. Even so, in the worst possible case where there are 720*4 hits in every packet generated (a hit rate we never expect to achieve), a sustained rate to the DCM of 27 kHz can still be achieved.

Component Deliverables

The proposed and achieved component deliverables for the FVTX project are shown in Table 4. As can be seen from the table, we have met all deliverables except the Working Spare FEM cards. We plan to order additional FEM cards with our remaining contingency to address this shortage. We also expect that since we have had some ROCs damaged during installation and commissioning that we will order some additional ROCs to address any future replacements that might be needed.

Table 4 Component Deliverables of FVTX.

Item	Number Proposed	Number Delivered	Working Spares Proposed	Working Spares Delivered
Wedge assemblies				
Large Sensors	288	288	25 in spare wedges	25
Small Sensors	96	96	8 in spare wedges	10
Large Wedges	288	288	25	25
Small Wedges	96	96	8	10
ROC boards	24	24	4	4

FEM boards	48	48	6	4
Mechanical				
Large ½ Disks	12	12	2	2
Small ½ Disks	4	4	1	1
Suspension system	1 (VTX funded)	1	0	0
Dry gas enclosure	1 (VTX funded)	1	0	0
Cooling system	1 (VTX funded)	1	0	0
Power supply system	1	1	Spare components available	2 conts. + 4 dist. cards
DCM channels	48	48	4	8

Detector Commissioning

We have been commissioning the detector since the installation in December 2011. In the below sections we cover the current status of the infrastructure systems needed to support the detector and the Data Acquisition performance which we have monitored during commissioning.

Cooling

The FVTX uses the same cooling system as the VTX, which was designed for both the VTX and the FVTX. Upon installation, the FVTX was connected up to the VTX/FVTX cooling system by PHENIX technicians. The cooling system has performed as designed. Based on experience from VTX running in RUN-11, a procedure has been put in place to monitor the NOVEC coolant for contamination on a regular basis and filter the NOVEC as needed. PHENIX technicians continue to follow the monitoring and filtering procedures on a weekly basis.

Bias Voltage

The bias system consists of a WIENER/ISEG MPOD system and FVTX designed bias distribution crate. The MPOD system provides 48 channels of regulated and monitored bias voltage. The FVTX bias distribution crate provides AC ground isolation and channel switching for the 384 wedge biases. The full system was installed and tested prior to the start of RUN-12. The control software is based on software that was developed for and used by the VTX system. Additional routines were developed by the FVTX group to control the FVTX bias distribution and are fully integrated with the MPOD control software. The system (hardware and software) was installed and tested prior to the start or RUN-12 and is currently fully functional.

Low Voltage

The FVTX detector uses the PHENIX Standard Voltage Distribution System based on bulk supplies from VICOR and custom designed distribution modules that provide switching and monitoring capabilities. This was augmented with FVTX LV distribution modules for the wedge low voltage distribution that provides independent switching and AC ground isolation for the 384 wedges. The system is divided into 2 separate systems, south cage and north cage. All bulk supplies, power distribution crates and racks were installed in the IR prior to the start of RUN-12. The software control of the PHENIX distribution system is via an ADAMS system that is used throughout PHENIX for slow control and monitoring. Additional software was provided by the FVTX group for control of the wedge distribution crates. All LV channels are currently functional.

Cabling

Cables for the bias, wedge low voltage and fiber optics were assembled and tested by outside vendors and delivered to PHENIX prior to the installation of the FVTX in the IR. ROC power cables and other miscellaneous cables were assembled by PHENIX technicians prior to installation into the IR. All cables were pulled and dressed in as part of the installation by PHENIX technicians.

Interlocks

The FVTX is part of the interlock system for the VTX. Power is interlocked on temperature and coolant flow. The interlocks were designed and implemented by the PHENIX engineering staff with assistance from an outside vendor. The interlock system was implemented at the start of RUN-12 and is fully functional with temperatures and flow rates logged in a regular basis.

Calibration System and Wedge Performance

The FVTX calibration system is used to quickly determine the state of each channel in the FVTX detector at a given time. The calibration system pulses the front end of each of the ~1 million channels with 64 different voltages. By analyzing the data that comes out of this voltage scan we can determine:

- Whether the full readout chain and slow control communication is operating for the channel
- The threshold for each channel
- The noise level of each channel. This is important for determining if we have any “hot” channels which should be masked off or if we have any dead channels

The calibration system has been exercised extensively during the commissioning of the detector and with it we have determined that all of the above measurements are within our specifications. The system is fully functional and we continue to take calibration data on approximately a daily basis to keep a record of the state of the detector during data collection.

Data Stream from Wedge to FEM

The unit element of the detector is the Wedge (each consists of one Silicon Sensor and a set of 10 or 26 FPHX chips). A set of 16 wedges connect via a set of extension cables to a single ROC (Read-Out Card) board located on the aluminum cooling disc surrounding the detector assembly. The ROC board contains 4 main data FPGAs which combine and process the serial data streams from the Wedges

and send them from the IR over the optical fibers; and one Slow Control FPGA designed to generate the clock signals for the wedges and control overall board functionality over the dedicated bi-directional slow control fiber link.

Each FPHX chip has 2 LVDS outputs running at 20 times the Beam Clock frequency Serial Clock (approximately 190 MHz). The overall instantaneous bandwidth for the full detector exceeds 3.2 Tb/s. It consists of more than 17,000 LVDS data lines that need to be readout, synchronized and sent out as fast as it possibly can in order to minimize the latency.

The ROC functionality had been rigorously tested to operate under worst possible conditions. It was able to process without interruptions the event when every strip on a particular Wedge side was pulsed by a test pulse. The board was able to operate without losing synchronization of the fiber optical links for days. The most critical for the data transmission components of the FPGA design have been built to be triple redundant to minimize any adverse effects of radiation next to the collision region.

A set of 768 optical fibers send the data from the ROC board to the Counting House where they connect to crates of FEM (Front-End Module) boards. The FEM board hosts a large scale data FPGA that buffers the data, sort them by the beam clock counter and combine the data from 4 individual FEM channels into a standardized PHENIX packet. All 4 FEM channels work in parallel and use 300 MHz internal clock to minimize the latency in the data path. Due to this, the overall bandwidth inside the FEM FPGA reaches 40 Gb/s and we have sufficient time to assemble and output within the required time limits even the most violent packet. Such tests had been successfully performed.

The secondary function of the FEM board is to send/receive the Slow Control fiber communication to/from the ROC board it controls. Also each FEM board holds an on-board EEPROM chip that stores the most up-to-data configuration of each and every FPHX chip associated with this particular FEM board. As a result, the download of all the parameters does not need to go through the slow control chain, but only needs a start pulse and takes milliseconds. This feature makes the FVTX detector very fast in terms of initialization despite the fact that it has

over 1 million of the readout channels.

PHENIX DCM Readout to Event Builder

The readout of the FVTX detector through the PHENIX DCMs and into the event builder is fully functional. We have established that we can read out the detector at a steady-state trigger rate of 7.9 kHz and observed no data loss or parity errors.

We also optimized the FVTX timing-delay so the FVTX will take data coherently with the PHENIX trigger. Because of the flexibility of the FVTX DAQ system, we can determine the optimal delay in a relatively short beam-time (5 minutes) by scanning the delay on the FEM as shown in Figure 8. At the optimal FEM delay, the FVTX will read a maximal amount of hits per trigger. Several such scans were performed throughout the run period and a consistent optimal delay was extracted, which showed that the timing for FVTX is very stable.

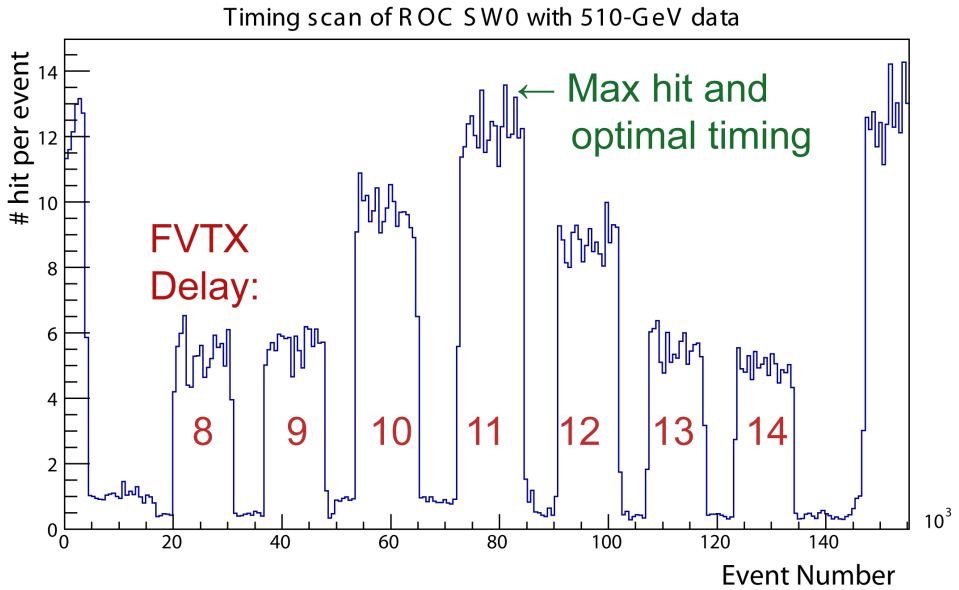

Figure 8 Hit versus event for ROC SW0 during a timing scan with 510-GeV p-p data. For each 10k events, FVTX delay was increased by one beam-clock (106 ns). The detector threshold was temporarily increased between each step to minimize the hit rate during the delay changes. At the optimal delay (FVTX delay of 11), the max number of hit per event was recorded. This analysis was repeated for other ROCs which showed a consistent optimal delay.

Contingency Spending Plan

At the completion of the FVTX project in December 2011 we had approximately $70k-$80k in contingency remaining. Part of this had already been converted to operations funds when FNAL returned remaining wedge assembly funds to BNL at the end of wedge assembly. With these funds, we plan to purchase additional spare parts for the FVTX detector system. Some of the spare parts we would like to purchase include:

- 6 FEM boards – quote = $20k
- LV Distribution board front panels = $5k
- Extra clock distribution boards ~$4k
- Extra ROC boards – quote estimate ~$15k/board